Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 6, with the following rewritten paragraph:

This application is a divisional of U.S. Serial No. 09/747,056 filed December 22, 2000, now U.S. Patent No. 6,704,857 ~~and~~ which claims the benefit of U.S. Provisional Application Serial No. 60/171,911 filed December 23, 1999 both of which ~~is~~ are incorporated by reference herein in ~~its~~ their entirety.

Please replace the paragraph beginning at page 3, line 16, with the following rewritten paragraph:

The present invention may be applicable to a variety of processing and array designs; however, an exemplary and presently preferred architecture for use in conjunction with the present invention is the ManArray™ architecture. Further details of a presently preferred ManArray core, architecture, and instructions for use in conjunction with the present invention are found in U.S. Patent Application Serial No. 08/885,310 filed June 30, 1997, now U.S. Patent No. 6,023,753, U.S. Patent Application Serial No. 08/949,122 filed October 10, 1997, now U.S. Patent No. 6,167,502, U.S. Patent Application Serial No. 09/169,255 filed October 9, 1998, now U.S. Patent No. 6,343,356, U.S. Patent Application Serial No. 09/169,256 filed October 9, 1998, now U. S. Patent No. 6,167,501, U.S. Patent Application Serial No. 09/169,072, filed October 9, 1998, now U.S. Patent No. 6,219,776, U.S. Patent Application Serial No. 09/187,539 filed November 6, 1998, now U.S. Patent No. 6,151,668, U.S. Patent Application Serial No. 09/205,588 filed December 4, 1998, now U.S. Patent No. 6,173,389, U.S. Patent Application

Serial No. 09/215,081 filed December 18, 1998, now U.S. Patent No. 6,101,592, U.S. Patent Application Serial No. 09/228,374 filed January 12, 1999, now U.S. Patent No. 6,216,223, U.S. Patent Application Serial No. 09/238,446 filed January 28, 1999, now U.S. Patent No. 6,366,999, U.S. Patent Application Serial No. 09/267,570 filed March 12, 1999, now U.S. Patent No. 6,446,190, U.S. Patent Application Serial No. 09/337,839 filed June 22, 1999 entitled "Efficient Complex Multiplication and Fast Fourier Transform (FFT) Implementation on the ManArray Architecture", U.S. Patent Application Serial No. 09/350,191 filed July 9, 1999, now U.S. Patent No. 6,356,994, U.S. Patent Application Serial No. 09/422,015 filed October 21, 1999, now U.S. Patent No. 6,408,382, U.S. Patent Application Serial No. 09/432,705 filed November 2, 1999, ~~entitled "Methods and Apparatus for Improved Motion Estimation for Video Encoding"~~now U.S. Patent No. 6,697,427, U.S. Patent Application Serial No. 09/471,217 filed December 23, 1999, ~~entitled "Methods and Apparatus for Providing Data Transfer Control"~~now U.S. Patent No. 6,260,082, U.S. Patent Application Serial No. 09/472,372 filed December 23, 1999, now U.S. Patent No. 6,256,683, U.S. Patent Application Serial No. 09/596,103 filed June 16, 2000, now U.S. Patent No. 6,397,324, U.S. Patent Application Serial No. 09/598,567 entitled "Methods and Apparatus for Improved Efficiency in Pipeline Simulation and Emulation" filed June 21, 2000, U.S. Patent Application Serial No. 09/598,564 filed June 21, 2000, now U.S. Patent No. 6,622,238, U.S. Patent Application Serial No. 09/598,566 ~~entitled "Methods and Apparatus for Generalized Event Detection and Action Specification in a Processor"~~ filed June 21, 2000, now U.S. Patent No. 6,735,690, and U.S. Patent Application Serial No. 09/598,084 filed June 21, 2000, now U.S. Patent No. 6,654,870, and U.S. Patent Application Serial No. 09/599,980 ~~entitled~~

~~"Methods and Apparatus for Parallel Processing Utilizing a Manifold Array (ManArray) Architecture and Instruction Syntax"~~ filed June 22, 2000, now U.S. Patent No. 6,748,517 all of which are assigned to the assignee of the present invention and incorporated by reference herein in their entirety.

Please replace the paragraph beginning at page 14, line 21, with the following rewritten paragraph:

The Fig. 6 VIM address adder functional blocks, as exemplified by ALU VIM address adder 604, are different than the adder functional block 504 as shown in Fig. 5 in order to support the VIM address increment capability required by the load VLIW-2 (LV2) instruction 455 of Fig. 4C as described in the syntax/operation block 460. This capability allows the instructions following the LV2 instruction to be loaded at:

(V[01]+VIMOFFS)[UnitVIM] $\leftarrow 1^{st}$ Instruction following LV2

(V[01]+VIMOFFS+1)[UnitVIM] $\leftarrow 2^{nd}$ Instruction following LV2

:

(V[01]+VIMOFFS+InstrCnt)[UnitVIM] $\leftarrow$ (InstrCnt+1)th Instruction following LV2

The instruction count parameter InstrCnt is a binary coded number, 0 thru F, that represents from 1 to 16 instructions that can be loaded into up to 16 consecutive UnitVIM locations.